AMENDMENT OF THE CLAIMS

The following listing will replace all prior listing of claims in the application.

Listing of Claims:

1. (Currently amended) A method of fabricating a die containing an integrated circuit comprising active components and passive components, at least a part of the passive components comprising critical passive components, ~~wherein production of the critical passive components necessitates the use of a first temperature higher than a second temperature above which the active components are unacceptably degraded,~~ the method comprising:

producing a first substrate including at least one active component including heating the first substrate at a temperature lower than a first temperature above which the first substrate is unacceptably degraded; ~~and~~

producing a second substrate including the critical passive components ~~by using~~ including heating the second substrate at a temperature higher than the first temperature;

bonding the first and second substrates, wherein the bonding comprises performing a layer transfer; and

after bonding of the first and second substrates, producing at least one interconnection line between the components of ~~said~~ the first and second substrates, ~~said~~ the interconnection line passing through the second substrate.

2. (Currently amended) A method according to claim 1, wherein ~~said~~ the at least one active component comprises transistors.

3. (Currently amended) A method according to claim 1, wherein ~~said~~ the critical passive components comprise at least one capacitor and at least one microelectromechanical system (MEMS).

4. (Currently amended) A method according to claim 1 wherein ~~said~~ the critical passive components comprise at least one capacitor or at least one microelectromechanical system (MEMS).

5. (Currently amended) A method according to claim 3, wherein a dielectric material of ~~said~~ the at least one capacitor comprises a perovskite.

6. (Currently amended) A method according to claim 1, wherein producing ~~said~~ the second substrate comprises producing an electrically conductive material.

7. (Currently amended) A method according to claim 1, wherein producing ~~said~~ the second substrate comprises producing a dielectric material.

8. (Currently amended) A method according to claim 7, wherein producing ~~said~~ the second substrate comprises producing perovskite.

9. (Currently amended) A method according to claim 1 further comprising producing dielectric insulation trenches in ~~said~~ the second substrate during the production of ~~said~~ the second substrate.

10. (Currently amended) A method according to claim 1 further comprising producing at least one non-critical passive component during the production of ~~said~~ the second substrate.

11. (Previously presented) A method according to claim 10, wherein producing the non-critical passive component comprises producing a capacitor in trenches.

12. (Currently amended) A method according to claim 9 further comprising producing at least one inductor in the vicinity of a face of the second substrate opposite a bonding face after ~~said~~ the bonding of the two substrates.

13. (Currently amended) A method according to claim 12 further comprising producing ~~said~~ the at least one inductor on ~~said~~ the dielectric insulation trenches.

14. (Cancelled)

15. (Previously presented) A die fabricated by a method according to claim 1.

16. (Currently amended) A die made of a single stack of layers, containing an integrated circuit comprising active components produced at a temperature lower than a first temperature above which the active components are unacceptably degraded and comprising passive components ~~and including a single stack of layers~~,

wherein at least a part of the passive components comprising critical passive components produced at a temperature higher than the first temperature above which the active components are unacceptably degraded, ~~wherein production of the critical passive components necessitates the use of a first temperature higher than a second temperature above which the active components are unacceptably degraded,~~

wherein ~~said~~ the die comprises an interface between two of ~~said~~the layers such that a first portion of the die situated on one side of ~~said~~ the interface includes ~~at least one~~the active component ~~of said active components~~ and a second portion of ~~said~~ the die situated on the other side of the interface includes the critical passive components produced at the temperature higher than~~of said passive components produced at or said~~ the first temperature,

wherein the die ~~comprising~~ comprises at least one interconnection line between the components of ~~said~~ the first and second portions, ~~said~~the interconnection line passing through the second portion of the die.

17. (Currently amended) A die according to claim 16 wherein ~~said~~ the critical passive components comprise at least one capacitor and at least one MEMS enclosed in a cavity situated inside ~~said~~ the die.

18. (Cancelled)

19. (Previously presented) A die according to claim 17, wherein the at least one capacitor comprises a dielectric material comprising perovskite.

20. (Currently amended) A die according to claim 16, wherein ~~said~~ the die further comprises dielectric insulation trenches.

21. (Currently amended) A die according to claim 16, wherein ~~said~~ the integrated circuit further comprises at least one non-critical passive component.

22. (Currently amended) A die according to claim 21 wherein ~~said~~t he non-critical passive component comprises a capacitor in trenches.

23. (Currently amended) A die according to claim 16, wherein ~~said~~ the active components are disposed in the vicinity of a first face of the die and wherein ~~said~~ the integrated circuit further comprises at least one inductor situated in a vicinity of ~~said~~ the face of the die opposite ~~said~~ the first face.

24. (Currently amended) A die according to claim 23, wherein ~~said~~ the at least one inductor is situated on inductive insulation trenches.

25. (Currently amended) A die according to any one of claim 16, wherein ~~said~~ the active components are disposed in a vicinity of a first face of ~~said~~ the die and ~~said~~ the die further comprises at least one interconnection line that emerges in the vicinity of ~~said~~ the face of ~~said~~ the die opposite ~~said~~ the first face.

26. (Currently amended) A die according to any one of claim 21 wherein ~~said~~ the active components are disposed in a vicinity of a first face of ~~said~~ the die and ~~said~~ the die further comprises at least one interconnection line that emerges in the vicinity of ~~said~~ the face of ~~said~~ the die opposite ~~said~~ the first face.

27. (Currently amended) A method according to claim 13, wherein ~~said~~ the at least one inductor and at least one of ~~said~~ the interconnection lines are produced during a same process step.

28. (Currently amended) The method according to claim 1, wherein the ~~second~~ first temperature is about 450°C.

29. (Previously presented) The method according to claim 1, wherein producing the first substrate comprises producing a substrate including all of the active components of the integrated circuit, and wherein producing the second substrate comprises producing a substrate including only passive components.

30. (Currently amended) The method according to claim 1, wherein producing the first substrate further comprises producing the at least one active component comprising an interconnect metal that ~~may be~~ is unacceptably degraded at a temperature above the first temperature.